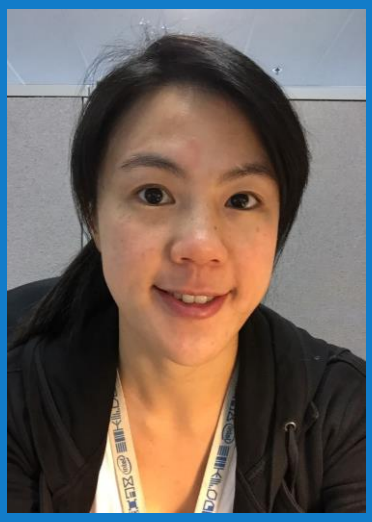
Intel PhD Tech Talk:
Intel's Silicon process technology with an emphasis on scaling electronic devices

Date: Wednesday, June 24th
Time: 6:00 pm
Location: Seeley G. Mudd (SGM) 101

Food Provided
Please Bring
Your Resume!

Join Jocelyn Lee, PhD (USC alumna) and Jeff Birdsall for a discussion on cutting edge developments and opportunities within Intel's Logic Technology Development Group.



Dr. Jocelyn Lee is a Ramp Litho Track Group Leader in Intel's Logic Technology Development organization. She joined Intel five years ago after earning her B.S. in Chemical Engineering from UC Berkeley and her PhD, also in Chemical Engineering, from USC. Her current role is focusing on the development and manufacturing ramp in the under-layer coating process.

Jeff Birdsall is an Engineering Manager and has spent over 19 years at Intel. He directs several areas of development and manufacturing ramp activities for Intel's cutting edge etch processes.

Immediate openings for grad students in the following disciplines:

Applied Physics
Chemical Engineering
Chemistry
Computer Engineering
Electrical Engineering
Materials Science
Mechanical Engineering

Interviews held Thursday, 6/25!

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